TSEP Technical Software Engineering Plazotta

Innovation made measurable.

Chronos V2.1

IEEE 1588-2019 PTP Stack

Time-synchronous processes are an essential topic in all areas of industry and especially in the areas of production, automation and measurement technology. The IEEE 1588 standard provides a protocol to synchronize the time understanding of different devices via an Ethernet network. Since the standard was published in 2002, it has been continuously developed. The TSEP product Chronos now also supports the new IEEE 1588-2019 standard from ver-sion 2.1 onwards. Chronos is available on various plat-forms (Windows / Linux / RTOSs) and supports Intel net-work chips (i210/i211 and i350). Chronos also contains a large number of tools, such as the visualization of time jitter, synchronization of the system time or the control and configuration of the IEEE 1588 topology via management messages. With the Chronos 2.1 version, in particular, a novel application of virtual boundary clocks is possible, which means that heterogeneous systems with different transport channels can now be implemented.

Highlights

- Supports IEEE 1588-2008 and 1588-2019
- Supports Windows, Linux and RTOS (IntervalZero/TenAsys)
- Supports Intel i210/i211 and i350
- Supports Ordinary, Boundary and Transparent Clocks
- OneStep und TwoStep Synchronisation
- Management Node
- User Defined Servo Algorithmen

High-Performance and Scalable Implementation

Chronos is TSEP's own implementation of the IEEE 1588 standard (PTP stack), which is implemented without any additional software (open source, 3rd party software). A particular focus of the stack was the interoperability and usability of the stack in a diverse topology. Chronos thus represents an IEEE 1588 software platform with which different operating systems and network architectures can be used with the IEEE 1588 standard. For time-critical applications portings from Chronos to real-time operating systems, such as, for example, from IntervalZero and TenAsys, are availables. The combination of the high accuracy Chronos and the deterministic behavior of an RTOS guarantees time-synchronous processing of events.

Chronos relies on network chips that support IEEE 1588 and are available for the consumer market, e.g. the Intel network chip families Intel I21x and I35x. TSEP is a partner of Intel and has access to the Intel network drivers and was able to optimize them accordingly for Chronos.

Chronos is tested and validated on internal reference systems and must demonstrate the necessary performance and the stability for the various combinations of OS and of different network chips, as it is necessary for a 24/7 application.

Servo Algorithm

General

Typically, clocks are implemented using a clock counter; modulation is carried out by adjusting the counting frequency and its value. It is technically not possible to generate identical and synchronous frequencies with several oscillators. This adaptation must be carried out using a complex control algorithm. IEEE 1588 tries to synchronize these free running clocks with the help of a defined protocol. However, the topology of the system has an influence on the system's parameters and thus on the control algorithm, so IEEE 1588 cannot define a default control algorithm.

Default Servo Algorithm

TSEP offers a configurable default algorithm for frequency adjustment, which is commonly referred to as servo. The servo only uses the determined time difference between master and slave (also called Offset) in order to determine the error in the frequency of your counter clock. This type of algorithm is independent of the hardware topology used and delivers useful results.

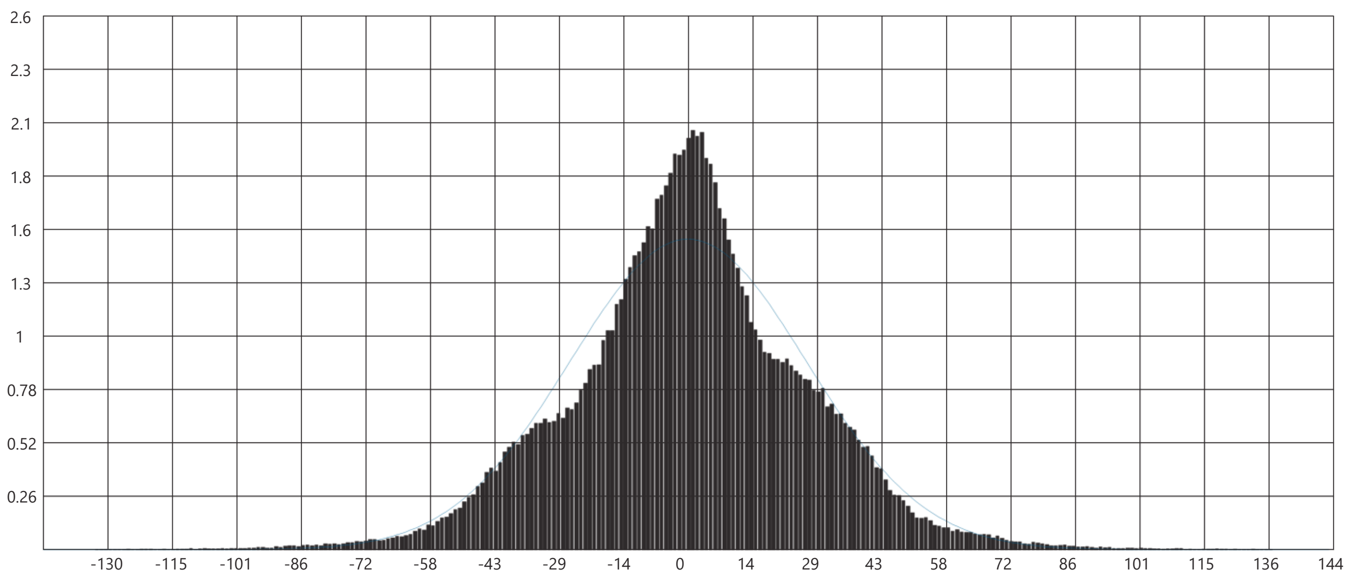
Customer Servo-Algorithm

Since every IEEE 1588 implementation is affected by the underlying hardware and hardware topology, there cannot be "the general control algorithm" and a custom servo algorithm may be more suitable or even required. This is why the Chronos servo algorithm is in its own library and so every customer can derive its own servo algorithm with the help of an interface class. Knowledge of the hardware used and the errors to be expected from the network topology can be incorporated into the calculation of the control variables.

Sources of Interferences

The data transmission in the Ethernet according to IEEE 802.3 is non-deterministic, every participant can access the network at any time (Aloha principle). This can result in packets being transmitted later than expected. Algorithms such as Kalman filters, which can be specifically modeled for the corresponding problem, are particularly suitable for this type of control and also in general..

Fig. 1: Distribution of the measured Offsets in nanoseconds during a long-term test with a reference system.



Native Boundary Clock Support

Since boundary clocks synchronize the time between at least 2 internal ordinary clocks, non-deterministic errors must be expected with pure software solutions. In order to minimize these deviations, TSEP has optimized the existing Intel drivers so that this synchronization is carried out within the driver. This way, operating system-specific errors can be minimized.

With the help of this approach, virtuell boundary clocks that use different transport layers can also optimally synchronize. In this way, high-precision boundary clocks can be implemented primarily on non-real-time systems. Thanks to the modular approach at Chronos, self-developed transport layers can also use this mechanism.

Modular Concept

TSEP Chronos was developed as a modular system due to the wide range of possible uses. The aim was to be able to adapt parts of the implementation to customer specifications. Chronos can therefore be easily adapted to customer requirements at any time. The modifications can either be carried out directly by the customer or the adaptation is provided directly by TSEP. The servo algorithm in particular has to be adapted to the customer requirements and the topology, which is why a customer-specific servo algorithm can be used in Chronos.

As defined in the standard, a "Best Master Clock Algorithm (BMCA) is implemented in Chronos, but this can be adapted for customers. The transport layer for communication can also be adapted to customer-specific requirements. "Ptp over IPV4, IPV6 and Ethernet" is currently supported. In order to achieve time synchronicity in the sub-nano seconds range, the time stamps must be made in the network hardware layer. As standard, Chronos can support the Intel network chips of the family I21x and I35x, but there are defined interfaces so that any hardware can be integrated.

PTP Profiles

Any external organization can create an IEEE 1588-compliant profile document for configuring a PTP implementation. The Chronos standard configuration is specified by the PTP profile of the LXI consortium. Chronos can also be configured for any other PTP profile with a Json file or via the PTP management messages. This Json file contains device-specific data, with the PTP profile configuration parameters and additional information that is used by the PTP stack during initialization.

```
"Restrictions":{
    "LogAnnounceInterval":{
       "Min":0,
       "Default":1,
       "Max":4
    },
    "LogSyncInterval":{
       "Min":-1,
       "Default":0,
       "Max":1
    },
```

Fig. 2: Snippet of a PTP-Profil

Time Synchronous Hardware Trigger

One of the use cases for IEEE 1588 is the generation of trigger signals to control actions and processes. The existing Intel network chips provide up to two trigger signals for this purpose. The possibilities of these trigger signals are, however, very limited; neither runtimes in the system nor the possibility of multiple trigger signals are provided. That is why TSEP has developed an IEEE 1588 trigger signal multiplexer which provides between 8 and 24 freely programmable trigger signals. This multiplexer takes into account, among other things, the runtime delays within the hardware and can thus correct the trigger signals accordingly. Both cyclic and single shot triggers are supported. The "IVI Trigger and Sync API" is available as an interface for programming.

Fig. 3: TSEP Themis with IEEE 1588 Trigger multiplexer

Management Node

TSEP Chronos supports all management messages defined by the IEEE 1588 standard and can act as a pure management node. This means that all clocks in a PTP domain can be configured using this mechanism and current performance data can be queried.

Both console-based tools and applications with a graphical user interface are available for the management messages. Future features should use this mechanism to display and manage the complete topology and the state of a Chronos instance.

Applications Scenarios

Automation and Production

A typical application of the IEEE 1588 PTP stack is in the field of automation and production. On the one hand, a precise common understanding of time is necessary for the coordination of machines in a system, so that all machines run as synchronously as possible. This increases the efficiency of the overall system and reduces the wear and tear on the components due to asynchronous movements. When testing and validating devices, a synchronized common time is also advantageous for reducing the latency between two sequential measurements. Ultimately, this leads to a reduction in the total production time per unit and thus to a higher production rate.

Distributed Measurement Systems

Alternatively, an IEEE 1588 PTP stack can be a critical component of a distributed measurement system. The synchronization of the internal clock of each device is an issue here, as the time information, when exactly a measured event occurred or has to be triggered, is important. However, if this system is distributed over a large distance, the runtime of the trigger signals in the cable and the drifting and poor long-term stability of the internal clocks of the end nodes reduce the accuracy of the information. A common understanding of time reduces the white noise and increases the correlation in the time-stamped data.

Upcoming Features

IEEE 1588-2019 Enhancements

There are major points of discussion in the IEEE 1588 standard about security. A proposal for the implementation of a security concept has already been included in the current standard. The discussions are still ongoing, but it is planned that an option for Chronos will be available in 2021 that contains a corresponding solution.

Real-Time Operating Systems

TSEP is continuously expanding the range of supported real-time operating systems (RTOS). The experience with the integration of our IEEE 1588 stack in different RTOS reduces the development time.

Time Sensitive Networking (TSN)

The TSN standard provides bandwidth regulation for communication via Ethernet. The IEEE 1588 standard serves as the basis for this. It is therefore planned to further develop Chronos in the direction of TSN, especially with regard to the proprietary real-time operating systems supported.

Order information

Binary licences

Order ref.	Description
CH-XXX	Deployment fee + n binary licenses
CH-100	Up to 100 binary licenses
CH-500	From 100 to 500 binary licenses
CH 1000	From 500 to 1000 binary licenses

General licences

Order ref.	Description
CH-PRO	Binary licenses + Support (3 years)
CH-INT	Integration + CH-PRO
CH-SUP	Support + Update (yearly)

TSEP
Technical Software Engineering Plazotta

For more information visit www.tsep.com or contact us.

Technical Software Engineering Plazotta

Hopfenstr. 30
85283 Wolnzach
Deutschland

Tel: +49 8442 96240 0
E-Mail: info@tsep.com