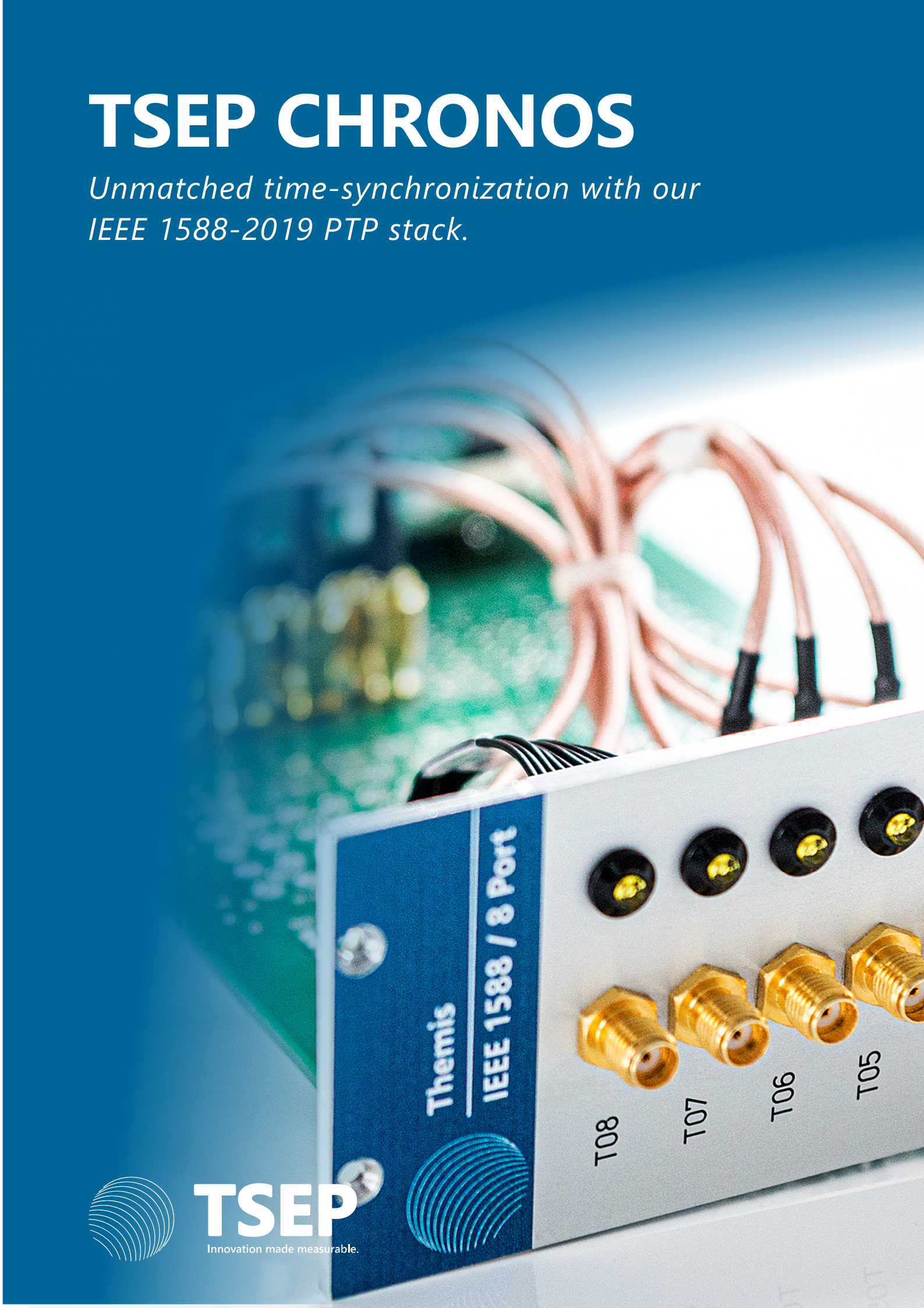
TSEP CHRONOS

Unmatched time-synchronization with our IEEE 1588-2019 PTP stack.



TSEP
Innovation made measurable.

TSEP Chronos

Our IEEE 1588-2019 PTP stack

Highlights

- Supports IEEE 1588-2008 and 1588-2019
- Supports Ordinary, Boundary and Transparent Clocks
- Supports Intel i210/i211 and i350
- Managing Node
- Supports Windows, Linux and RTOS (IntervalZero / TenAsys)
- User defined servo algorithm
- OneStep and TwoStep synchronization
- Timesynchronous Hardware Trigger

Time-synchronous processes are an essential topic in all areas of industry, and especially in the areas of production, automation and measurement technology. The IEEE 1588 standard provides a protocol to synchronize the time understanding of different devices via an Ethernet network. Since the standard was published in 2002, it has been continuously developed. The TSEP product Chronos now also supports the new IEEE 1588-2019 standard from version 2.0 onwards.

Chronos is available on various platforms (Windows / Linux / RTOSs) and supports Intel network chips (i210/i211 and i350). Chronos also contains numerous tools, such as the visualization of time jitter, synchronization of the system time or the control and configuration of the IEEE 1588 topology via management messages. With the Chronos 2.1 version, in particular, a novel application of virtual boundary clocks is possible, which means that heterogeneous systems with different transport channels can now be implemented.

High Performance and Scalable Implementation

TSEP Chronos is TSEP's own implementation of the IEEE 1588-PTP standard and focuses on the interoperability and usability in a diverse topology.

Platform Independence

A particular focus of TSEP Chronos was the availability and portability of the stack to an arbitrary ecosystem. So it was necessary to implement this IEEE 1588 stack without any dependencies to additional software, e.g. open source and 3rd party software. Chronos thus represents an IEEE 1588 software platform with which different operating systems and network architectures can be used with the IEEE 1588 standard.

Affordable Consumer Hardware

TSEP Chronos only relies on network chips that support IEEE 1588 and are available for the consumer market, e.g. the Intel network chip families Intel I21x and I35x and others. TSEP is a partner of Intel and has access to the Intel network drivers and was able to customize these drivers accordingly for the IEEE 1588 functionality used by TSEP Chronos.

Time-synchronous Hardware Triggers

The Precision Time Protocol achieves time synchronization of the internal hardware clock of each device. TSEP developed with the Chronos software platform a tooling to facilitate this synchronized time understanding and to generate time synchronous Hardware Triggers.

Real-time Capabilities

For time-critical applications ports from Chronos to real-time operating systems (RTOS), such as, for example, from IntervalZero and TenAsys, are available. The combination of the high accuracy synchronization of Chronos and the deterministic behaviour of an RTOS guarantees time-synchronous processing of events.

Reliability

TSEP Chronos is tested and validated on internal reference systems and must demonstrate the necessary performance and the stability for the various combinations of OS and of different network chips, as it is necessary for a 24/7 application.

Modular Concept

TSEP Chronos was developed as a modular system due to the wide range of possible uses and customer requirements. The aim was to be able to adapt or enhance parts of the implementation to customer specifications. Chronos can therefore be easily adapted to customer requirements at any time. The modifications can either be carried out directly by the customer, or the adaptation is provided directly by TSEP.

Servo Algorithm

The servo algorithm module has the most impact on the performance of an IEEE 1588 stack. A configurable default servo algorithm is provided with TSEP Chronos, which satisfies the most of our customers requirements. For more sophisticated examples, customer-specific servo algorithms can be developed and used in Chronos.

Best Master Clock Algorithm

As defined in the standard, a default "Best Master Clock Algorithm" (BMCA) is implemented in Chronos. In case, there is a need for a custom Best Master Clock Algorithm, TSEP Chronos offers the possibility to replace this module and to use a custom algorithm.

Transport Layers

The transport layer for communication can also be adapted to customer-specific requirements. "PTP over IPV4, IPV6 and Ethernet" is currently supported. In particular, TSEP Chronos natively supports also heterogeneous systems with different combinations of transport layers.

Timestamping Layers

In order to achieve time synchronicity in the nano seconds range, the time stamps must be made in the network hardware layer. As standard, Chronos supports the Intel network chips of the family I21x and I35x, and by implementing further add-ons via the Chronos interfaces, any hardware with timestamping functionality can be utilized.


Themis
Power Unit
Themis
CPU Unit
Themis
IEEE 1588 / 8 Por
Themis
Vers: xx.xx
State: Starting
IP: 0.0.0.0
POWER
LAN STATUS
RESET
LCI
LAN2
LAN1
T08
T07
T06
T05
T04
T03
T02
T01

"TSEP CHRONOS IMPLEMENTS TIME SYNCHRONIZATION TO A VARIOUS AMOUNT OF PLATFORMS AND DEVICES VIA PTP."

Beyond Ordinary Clocks

TSEP Chronos offers unique features to act as a virtual boundary clock or management node.

Heterogeneous Systems

Within the IEEE 1588 Standard, PTP Instances with more than one Port are called Boundary Clocks. The new IEEE 1588-2019 standard explicitly specifies a media dependent abstraction layer such that each port within a Boundary Clock can be connected to a different transport layer, e.g. Ethernet, USB, CANBus, etc. This mechanism enables IEEE 1588-2019 compliant implementations to distribute the time-understanding over heterogeneous PTP networks. Additionally, thanks to the modular approach at Chronos, self-developed transport layers can also be used to set up a custom heterogeneous PTP network.

Management Node

TSEP Chronos supports all management messages defined by the IEEE 1588 standard and can act as a pure management node. This means that all clocks in a PTP domain can be configured using this mechanism and current performance data can be queried.

Both console-based tools and applications with a graphical user interface are available for the management messages. Future features should use this mechanism to display and manage the complete topology and the state of a Chronos instance.

Virtual Boundary Clock

Since boundary clocks synchronize the time between at least 2 internal ordinary clocks, non-deterministic errors must be expected with pure software solutions. In order to minimize these deviations, TSEP has optimized the existing Intel drivers so that this synchronization is carried out within the driver. This way, timing errors induced by the OS can be minimized. With the help of this approach, virtual boundary clocks that use different transport layers can also optimally synchronize. In case the used timestamping layer comprises generating and timestamping of hardware-triggers, this approach can be optimized even further.

System Clock Synchronization

By definition, implementations of the IEEE 1588 Standard only synchronize the clock module on the actual hardware. The system clock of the operating system is independent of the clock synchronization mechanism. Under some circumstances, it is required to perform an additional synchronization step between the hardware and the system clock. For this task, TSEP offers a separate tool. The tool accesses the synchronized time on the hardware and performs the time adaption with the TSEP Chronos default servo.

Flexbile Configuration&Monitoring

Adjust TSEP Chronos to your requirements and monitor all needed performance indicators!

Configuration

TSEP Chronos provides a variety of configuration possibilities to meet the needs of the user. The configuration parameters allows to adjust the different modules:

- PTP Profile
- Instance
- Ports
- Optional Features

The Chronos.Configurator with its GUI provides a straightforward approach for creating a configuration. With this tool the user can inspect and adjust the configuration step by Step.

Monitoring

Especially during an evaluation and integration phase of an IEEE 1588 stack it is crucial to monitor certain parameters. TSEP Chronos provides an interface to access the following information:

- State
- Traffic
- Performance
- Synchronization
- Management Message

For a better visualization of the monitored information a Graphical User Interface is provided.

PTP Profiles

Any external organization can create an IEEE 1588-compliant profile document for configuring a PTP implementation. The TSEP Chronos standard configuration is specified by the PTP profile of the LXI consortium. Chronos can also be configured for any other PTP profile with a JSON file or via the PTP management messages. This JSON file contains device-specific data, with the PTP profile configuration parameters and additional information that is used by the PTP stack during initialization. Commonly used and supported PTP-Profiles are:

- AES67 Standard
- SMPTE ST 2059-2 Standard
- IEEE C37.238-2017 Standard

```
42 "Restrictions":{
43   "LogAnnounceInterval":{
44      "Min":0,
45      "Default":1,
46      "Max":4
47   },
48   "LogSyncInterval":{
49      "Min":-1,
50      "Default":0,
51      "Max":1
52   },
```

Fig. 1: Snippet of a PTP-Profil

Understanding the Servo Algorithm

The performance of each IEEE 1588 implementation is measured by the accuracy of the time synchronization. A key component is the Servo Algorithm.

General

Typically, digital clocks are implemented using a fixed tick frequency, a time counter, and a tick increment. The time counter is incremented each tick interval by the value of the tick increment. A modulation of the clock is carried out by adjusting the tick increment and the time counter. It is technically not possible to generate identical and synchronous clocks, since the tick frequencies of several oscillators differ. IEEE 1588 provides a defined protocol to synchronize these free running clocks, and continuous adaptations must be carried out using a complex control algorithm. Since the topology of the system has an influence on the system's parameters and thus on the control algorithm, the IEEE 1588 cannot define a default control algorithm.

Default Servo Algorithm

TSEP offers a configurable default algorithm for clock time and clock frequency adjustment, which is commonly referred to as servo. The servo uses all time information available in the determined time difference between master and slave (also called Offset) in order to determine the error in the frequency of your counter clock. This type of algorithm is independent of the hardware topology used and delivers useful results. The servo also provides the capabilities to fine-tune certain parameters to achieve an optimal performance in the time synchronization process.

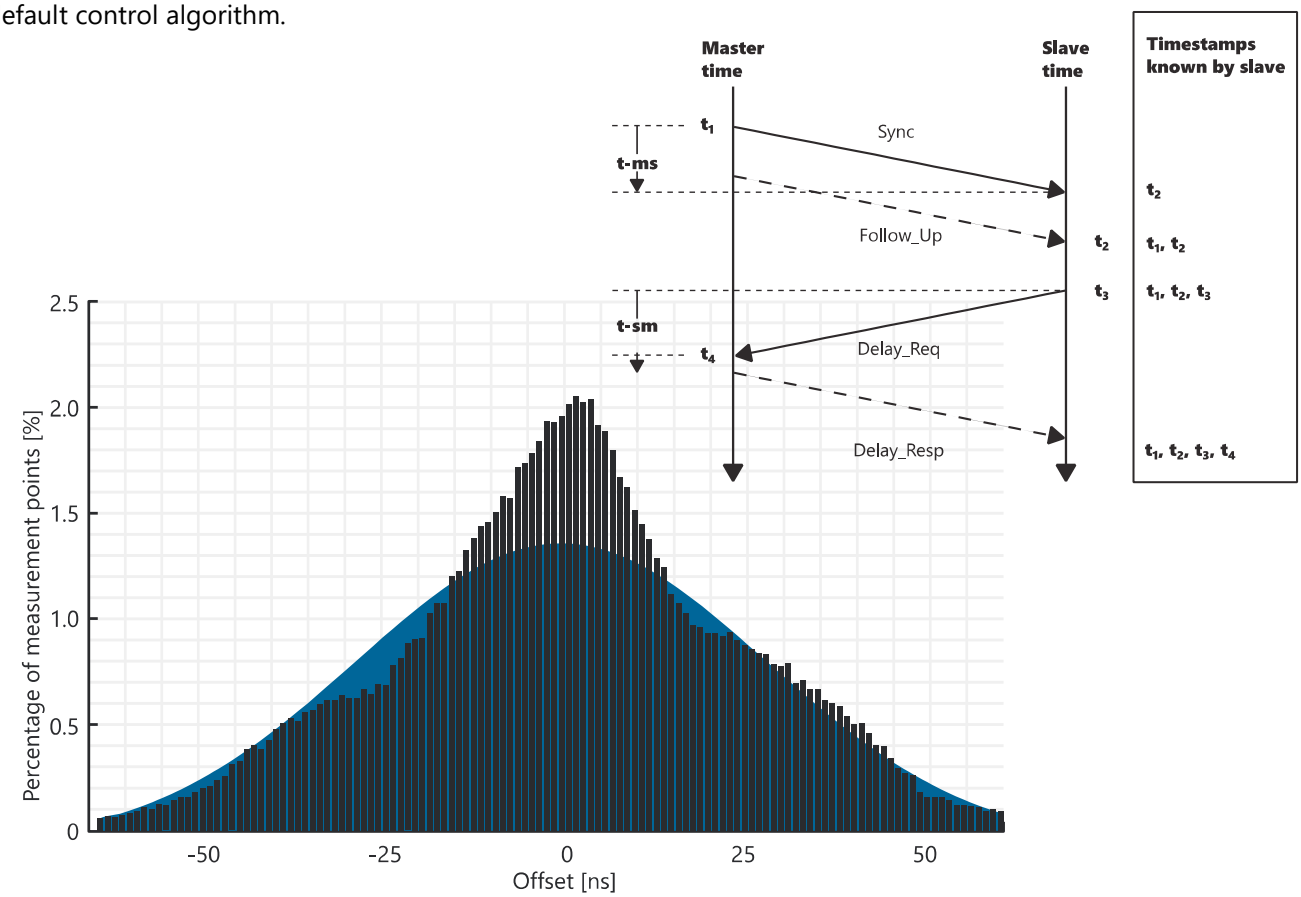


Fig. 2: Left: Distribution of the measured Offsets in nanoseconds during a long-term test with a reference system. Right: The precision time protocol.

Customer Servo Algorithm

Since every IEEE 1588 implementation is affected by the underlying hardware and hardware topology, there cannot be "the general control algorithm" and a custom servo algorithm may be more suitable or even required. This is why the software platform TSEP Chronos provides a servo algorithm interface such that every customer can implement its own servo algorithm. The derived servo algorithm can comprise the knowledge of the used hardware and the expected errors from the network topology, and to incorporated these information into the calculation of the control variables.

Sources of Interferences

The data transmission in the Ethernet according to IEEE 802.3 is non-deterministic, every participant can access the network at any time (Aloha principle). This can result in packets being transmitted later than expected. Additional different network traffic loads can yield to a delay of transmission and processing of Ethernet packages. These non-deterministic delays can yield to a single, overestimated mean path delay and offset. Regular servo algorithms rely on an almost constant mean path delay and these servos tend to overestimate the adaption. Algorithms such as Kalman filters can be specifically modelled for the corresponding problem and are particularly suitable for this type of control and also in general.

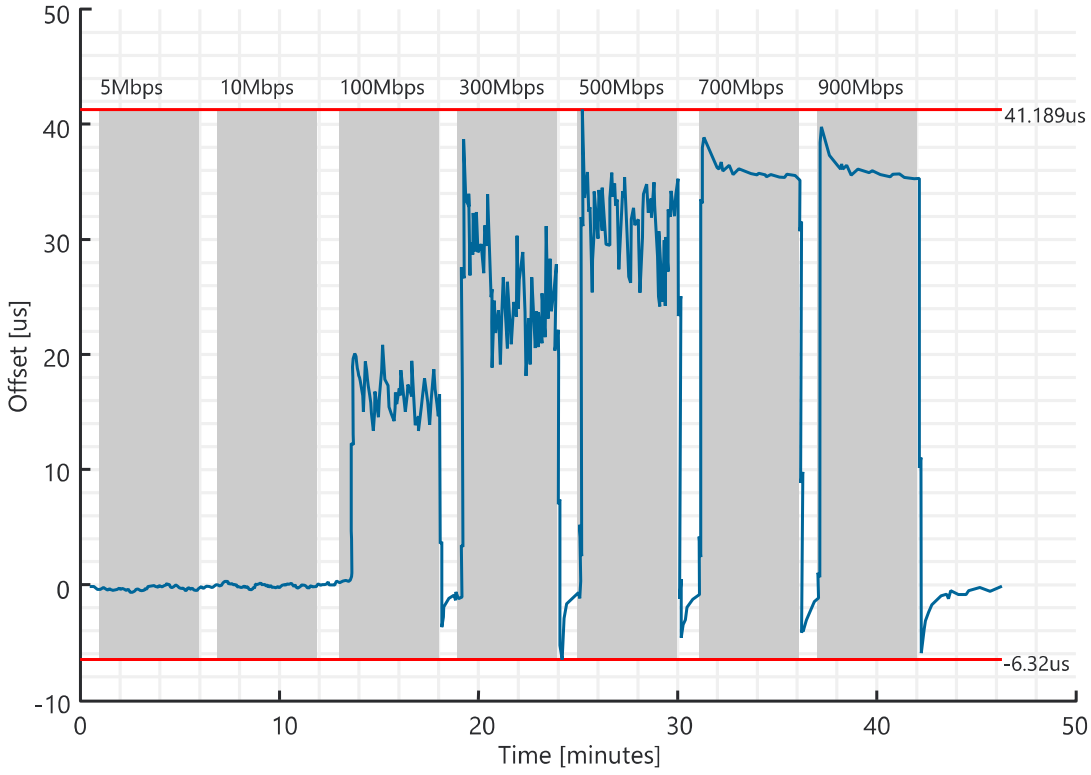


Fig. 3: Measured Offsets in microseconds during an Ethernet high-traffic test with various traffic loads where an uncalibrated servo algorithm is used.

Timesynchronous Hardware Trigger

Generate time-based trigger signals with your synchronized hardware to provide a precise time.

Utilizing Time

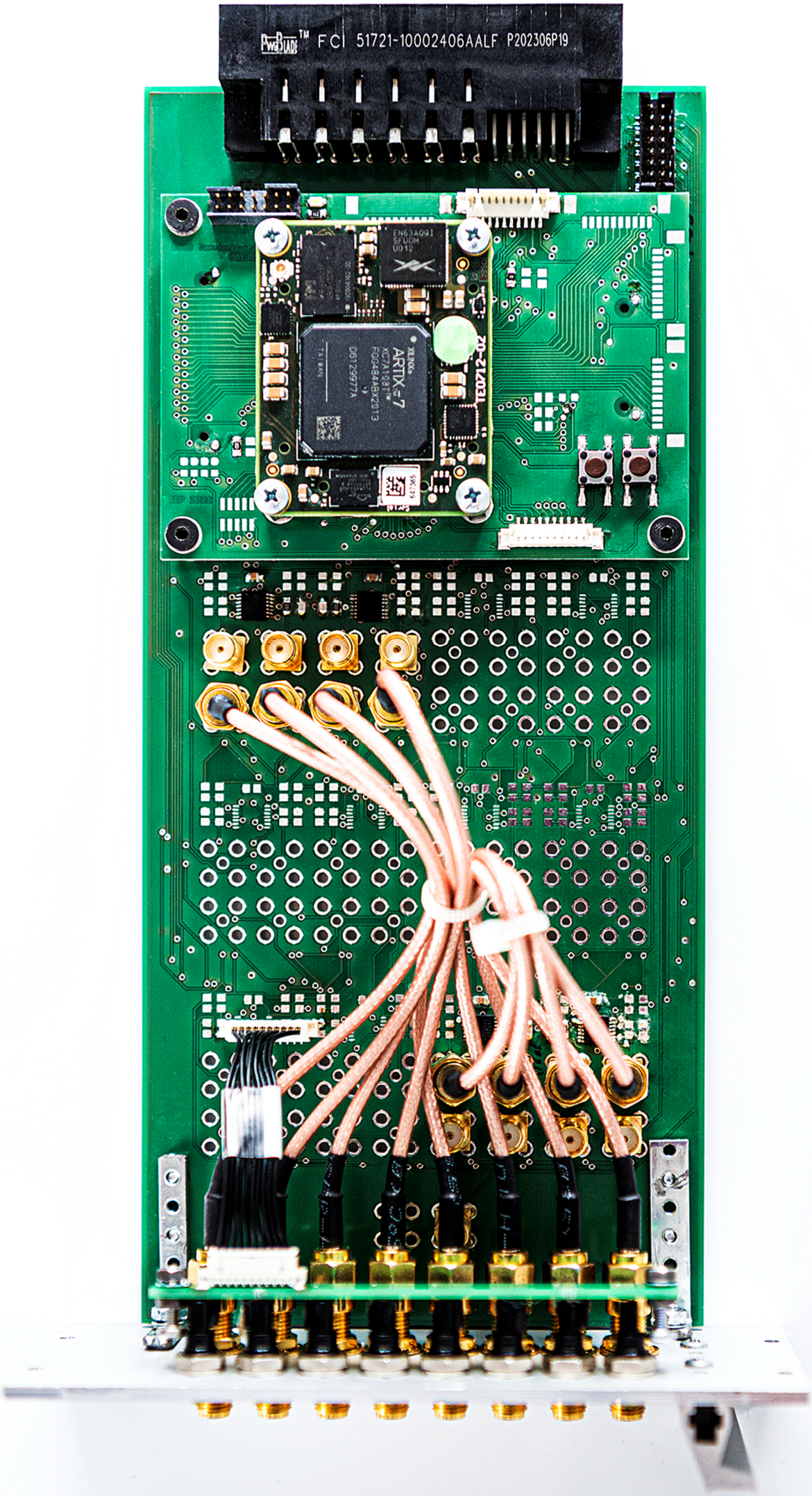
The key cause of using the IEEE 1588 PTP synchronization mechanism is to utilize the precisely synchronized time to control actions and processes in timing-crucial applications on the synchronized devices. These actions can be passive, such as timestamping during data acquisition and capturing an event at a scheduled moment. Also, active deterministic triggering of scheduled tasks and external devices is required to greatly increase the efficacy of the system. These triggers can be generated from two different sources. The first is initiated by a software (futures), the operating system (events), or the driver (interrupts). The second is a hardware trigger in the form of an electrical signal generated inside the microcontroller. The benefits of the hardware trigger compared to the software triggers is the deterministic nature of a microcontroller or a FPGA, which yields to decreased variation and delay in the execution of the operation. In contrast, software triggers heavily suffer from the non-deterministic scheduling and execution of task in an operating system such that the fluctuation are in the milliseconds range. Beside these effects, the accessibility of the clock module and the stored time information is an issue. For example, when timestamping data, the acquisition of the data can take place on a different bus than the PTP network is connected to. Moving the time information from one bus to another introduces additional variance to the accuracy of the timestamp.

TSEP Chronos

Here at TSEP, we incorporated all these functionalities inside the software Platform TSEP Chronos and defined custom PTP management messages to configure and access those. To achieve the best performance for Software triggers, we at TSEP decided to enhance the driver to create a direct access to the hardware clock and to reduce all latencies originating from the operating system. Additionally, hardware triggers for generating electrical output signals can be configured and this either remotely with PTP management messages or directly through the driver access. Currently, this functionality is supported for the Intel network interfaces chip families i21x and i350, since only these NICs support the desired requirements. Extension to other hardware is always possible, due to the modularity of TSEP Chronos.

Themis 1588 Multiplexer

The capabilities of these hardware trigger signals are, however, very limited. The Intel NICs only support two simple rectangular signals; multiple or complex trigger signals are not provided. That is why TSEP has developed an IEEE 1588 trigger signal multiplexer, which provides between 8 and 24 freely programmable trigger signals. This multiplexer takes into account, among other things, the runtime delays within the hardware and can thus correct the trigger signals accordingly. Both cyclic and single shot triggers are supported. The "IVI Trigger and Sync API" is available as an interface for programming.


FCI 51721-10002406AALF P202306P19
ARTIX-7
XC7A100T
TAIWAN

Enable T&M Devices with IEEE 1588

Combine the power of digital time synchronization with the world renowned specifications of the IVI Foundation.

The Missing Part in the IEEE 1588 Standard

The IEEE 1588 standard focuses on the distribution of a common time-understanding among all participants of a network. In the IEEE 1588-2008 there is no application interface defined to utilize the synchronized time, and even in the IEEE 1588-2019 only clock sinks and clock sources are defined. However, these modules are not sufficient to meet the requirements of the T&M industry. Also, no extension for time based trigger modules exists in the current version of the standard.

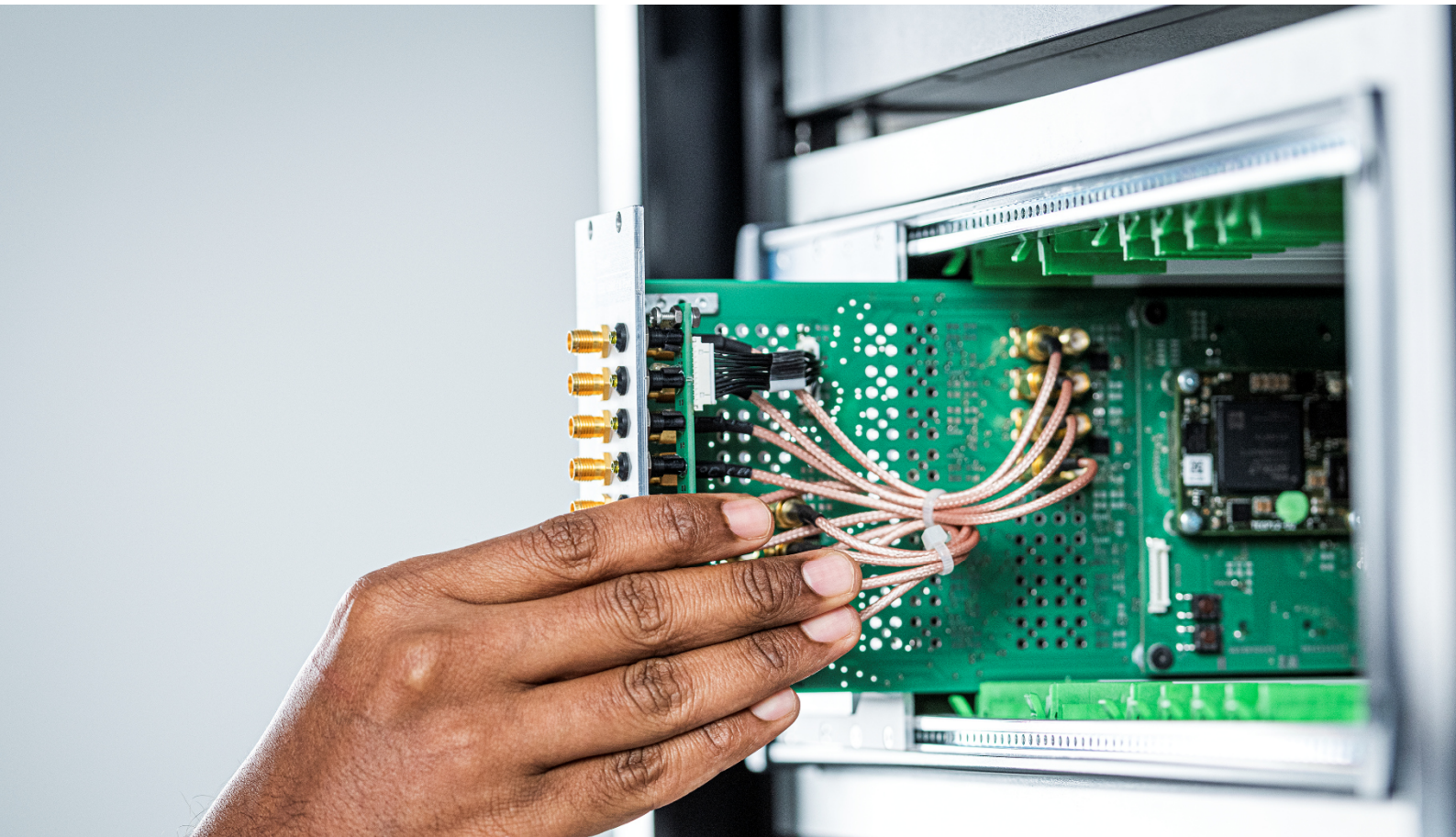
The largest benefit for the T&M industry would be if all devices in a test system supports a common IEEE 1588 API to simplify the interchangeability and increase the interoperability. This API must be supported by the leading manufacturer of measurement devices.

The IVI_LXI_SYNC Specification

The Interchangeable Virtual Instruments Foundation (IVI Foundation) published in cooperation with the LAN eXtensions for Instrumentation consortium (LXI) the IVI_LXI_SYNC specification to promote an interface which is compliant with common time-based operations for test and measurement devices. This specification is available for all members of the IVI Consortium, compatible with IVI drivers and stable since 2018.

The IVI_LXI_SYNC specification includes the missing requirements from the IEEE 1588 standard, i.e.:

- Expose functionality for access to the 1588 time base of the port.
- Definition of signal triggering with arm and trigger mechanism
- Definition of time based trigger, called alarms
- Definition of outbound events
- Logging mechanism to monitor the processing of the trigger and alarms



IMPROVE YOUR PRODUCT THROUGH MORE PRECISE MEASUREMENT TECHNOLOGY.

Knowledge Base

The IEEE 1588 Standard is a powerful tool for time synchronization. We share our knowledge to increase the insight in this topic.

Performance Measurement

During the evaluation of an IEEE 1588 stack there are to key performance indicators to measure: the compliance with respect to the IEEE 1588 Standard and the accuracy of the time synchronization. The first can be tested with dedicated test systems, which interacts with the IEEE 1588 Stack in a predefined way. For example, such a test system is realized in TSEP Kerberos 1588 Extension. The measurement of the accuracy of the time synchronization in a simplified system with only one Master Clock and one directly connected Ordinary Clock can be done in two different ways. First, the time offset in each synchronization cycle can be logged and visualized. Second, the Puls-Per-Second method is used. For this, both clocks have to emit an electrical signal that has a width of one second and a sharply rising edge that repeats once per second. These two signals are evaluated with a modern oscilloscope. The distance between the rising edges yields the true accuracy of the time-synchronization between Master Clock and Ordinary Clock. This scenario of one Master Clock and one Ordinary Clock can be arbitrarily extended, e.g. more boundary clocks or additional load on the Ethernet network.

Calibration is Key

In today's Test&Measurement systems the calibration is crucial for the performance of the measurement. Generally speaking, the higher the quality of the T&M equipment is, the more extensive is the effort spend on calibration. In time-based measurement scenarios, the common time-understanding is a crucial component for the quality of the measurement result. With the default configurations of the IEEE 1588 PTP stack reasonable accuracies for the time-synchronicity can be achieved. With new technologies like the 5G telecommunication standard, the need for a more restrictive time synchronicity is inevitable. Hence, it should be clear, that also the time synchronization process has to be part of the calibration procedure.

Absolute Time is not Important, Relative is!

A generic requirement for the usage of the time synchronization with a distributed network is the synchronization to a specific time zone, e.g. UTC or GMT+1. To achieve this link to an absolute time, additional hardware is needed to connect to the global NTP network and to distribute the absolute time in the PTP network. However, this introduces a systematically time-error in the PTP network, which is of the same magnitude as the synchronization error of the NTP network, i.e., in the millisecond's region. This error compromises the capability of time-synchronization accuracy of PTP drastically, which is in the nanosecond's region. Therefore, PTP has to been seen as a local time synchronization method where relative time matters and NTP has to been seen as a global one. A solution to this requirement is to synchronize a stable Master Clock in the beginning of the measurement to the absolute time with NTP. During the measurement, the Master Clock is disconnect to the NTP network and free running. After the measurement task is performed, the time of the Master Clock is compared to the absolute time and a global correction of the relative time in the system can be applied.

Identical Clocks are not Equal!

A common misunderstanding is the fact, that the internal clocks on identical Hardware are equal. In this context, equality means long term stability of the internal time with respect to a very precise (atomic) clock. However, there are multiple effects which impacts the stability. First, it could be shown, that inaccuracy and tolerances in the production of the silicon oscillators can affect the stability of the internal time. Second, the ambient temperature has also an impact on the oscillation frequency of the internal silicon oscillator and hence on the stability. Last, even the circuits on the chip can have an impact on the stability, since the trigger signal has to pass through these and this can distort the output signal..

Applications Scenarios

The IEEE 1588 Standard is already used in a broad field of applications. Can you find your application, too?

Automation and Production

A typical application of the IEEE 1588 PTP stack is in the field of automation and production. On the one hand, a precise common understanding of time is necessary for the coordination of machines in a system, so that all machines run as synchronously as possible. This increases the efficiency of the overall system and reduces the wear and tear on the components due to asynchronous movements. When testing and validating devices, a synchronized common time is also advantageous for reducing the latency between two sequential measurements. Ultimately, this leads to a reduction in the total production time per unit and thus to a higher production rate.

Distributed Measurement Systems

Alternatively, an IEEE 1588 PTP stack can be a critical component of a distributed measurement system. The synchronization of the internal clock of each device is an issue here, as the time information, when exactly a measured event occurred or has to be triggered, is important. However, if this system is distributed over a large distance, the runtime of the trigger signals in the cable and the drifting and poor long-term stability of the internal clocks of the end nodes reduce the accuracy of the information. A common understanding of time reduces the white noise and increases the correlation in the time-stamped data.

Upcoming Features

TSEP drives the development of TSEP Chronos further to meet with all customer requirements from today and tomorrow.

IEEE 1588-2019 Enhancements

There are major points of discussion in the IEEE 1588 standard about security. A proposal for the implementation of a security concept has already been included in the current standard. The discussions are still ongoing, but it is planned that an option for Chronos will be available that contains a corresponding solution.

Real-Time Operating Systems

TSEP is continuously expanding the range of supported real-time operating systems (RTOS). The experience with the integration of our IEEE 1588 stack in different RTOS reduces the development time.

Next-Generation Intel Network-Chips

The next generation Intel network interface chip families like the x540 and x550 also supports the IEEE 1588 standard. TSEP is planning to enable all PTP capabilities also with this consumer available hardware.

Time Sensitive Networking (TSN)

The TSN standard provides bandwidth regulation for communication via Ethernet. The IEEE 1588 standard serves as the basis for this. It is therefore planned to further develop Chronos in the direction of TSN, especially with regard to the proprietary real-time operating systems supported.

Sub-Nanosecond Accuracy

TSEP plans to push the boundaries of the accuracy of the time synchronicity with PTP. For this TSEP develops new hardware and software based on the PTP standard to achieve time accuracy in the ~100 picoseconds region.

Order Information

General License

Order ref.	Description
CH-PRO	Deployment fee
CH-BIN	Up to 100 binary lincenses
CH-SRC	From 100 to 500 licenses

Support + Update

Order ref.	Description
CH-SUP	Support + Update (1 year)
CH-SUP3	Support + Update (3 years)
CH-SUP5	Support + Update (5 years)

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About Us

Technical Software Engineering Plazotta GmbH

TSEP is a worldwide operating system house. For more than 30 years, we have successfully specialized in the development of system-related software and hardware in the fields of communications engineering, automotive, tele-communications, and measurement technology.

TSEP Chronos

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